We claim:

1. A method of forming a MOS transistor on a semiconductor substrate, comprising;

(a) providing a substrate having isolation regions and an active region formed therebetween, said active region has a gate dielectric layer formed thereon and a gate electrode with two sides on the gate dielectric layer;

(b) forming a temporary sidewall spacer on opposite sides of the gate electrode;

(c) forming a temporary etch stop layer between an isolation region and an adjacent temporary sidewall spacer;

(d) removing said temporary sidewall spacers and replacing with permanent sidewall spacers;

(e) implanting impurity ions in said gate electrode, permanent sidewall spacers, etch stop layer, and in the substrate in the active region and performing a rapid thermal anneal (RTA) to activate shallow source/drain regions and deep source/drain regions in said active region,

(f) removing the temporary etch stop layer to expose portions of the substrate; and

(g) forming a metal silicide layer on the exposed portions of substrate, permanent sidewall spacers, and on the gate electrode.

2. The method of claim **1** further comprised of forming a first sidewall spacer on opposite sides of the gate electrode before forming the temporary sidewall spacers.

3. The method of claim **2** wherein said first sidewall spacer is comprised of silicon oxide or silicon oxynitride having a width between about 150 and 200 Angstroms.

4. The method of claim **1** wherein said substrate is comprised of silicon and the gate electrode is polysilicon and has a thickness between about 1500 and 1800 Angstroms.

5. The method of claim **1** wherein said temporary sidewall spacers are comprised of silicon nitride having a width from about 1500 to 1600 Angstroms.

6. The method of claim **1** wherein said temporary etch stop layer is silicon oxide with a thickness from about 30 to 200 Angstroms and which is formed by a thermal oxidation in an O_2 ambient at a temperature between about 300^{o}C and 1000^{o}C.

7. The method of claim **6** wherein a thin oxide layer is formed on the gate electrode during said thermal oxidation and said thin oxide layer is subsequently removed during removal of the temporary etch stop layer.

8. The method of claim **1** wherein said permanent sidewall spacers are formed by depositing an amorphous silicon layer which is subsequently etched back.

9. The method of claim **8** wherein the substrate having said permanent sidewall spacers is annealed in a N_2 ambient to form crystalline silicon sidewall spacers before the implant step.

10. The method of claim **1** wherein said RTA step is performed by heating the substrate in a N_2 atmosphere at a temperature between about 900^{o}C and 1100^{o}C for a period between about 7 and 13 seconds.

11. The method of claim **1** wherein the metal deposited on said substrate to form a silicide is titanium or one or more of Ni, Co, W, Ta, Pt, Er, Hf, Al, and Pd.

12. A method of forming a PMOS and an NMOS transistor on a semiconductor substrate comprising the steps of:

(a) providing a substrate having isolation regions and a first active region with an n-well and a second active region with a p-well formed therebetween, said first and second active regions have a gate dielectric layer formed thereon and a gate electrode with two sides on the gate dielectric layer;

(b) forming a temporary sidewall spacer on opposite sides of the gate electrodes;

(c) forming a temporary etch stop layer between an isolation region and an adjacent temporary sidewall spacer;

(d) removing said temporary sidewall spacers and replacing with permanent sidewall spacers;

(e) implanting a p-type dopant in said gate electrode, permanent sidewall spacers, etch stop layer, and in the substrate in the first active region;

(f) implanting an n-type dopant in said gate electrode, permanent sidewall spacers, etch stop layer, and in the substrate in the second active region;

(g) performing a rapid thermal anneal to form shallow source/drain regions and deep source/drain regions in said first and second active regions,

(h) removing the temporary etch stop layer to expose portions of the substrate; and

(i) forming a metal silicide layer on the exposed portions of substrate, permanent sidewall spacers, and on the gate electrodes.

13. The method of claim **12** further comprised of forming a first sidewall spacer adjacent to the gate electrodes before forming a temporary sidewall spacer.

14. The method of claim **13** wherein said first sidewall spacer is comprised of silicon oxide or silicon oxynitride having a width between about 150 and 200 Angstroms.

15. The method of claim **12** wherein said substrate is comprised of silicon and the gate electrode is polysilicon and has a thickness between about 1500 and 1800 Angstroms.

16. The method of claim **12** wherein said temporary sidewall spacers are comprised of silicon nitride having a width from about 1500 to 1600 Angstroms.

17. The method of claim **12** wherein said temporary etch stop layer is silicon oxide which is formed by a thermal oxidation with an oxygen ambient at a temperature between about 300^{o}C and 1000^{o}C and has a thickness between about 30 and 200 Angstroms.

18. The method of claim **17** wherein a thin oxide layer is formed on the gate electrodes during said thermal oxidation and said thin oxide layer is subsequently removed during removal of the temporary etch stop layer

19. The method of claim **12** wherein said permanent sidewall spacers are formed by depositing an amorphous silicon layer which is subsequently etched back.

20. The method of claim **19** wherein the substrate having said permanent sidewall spacers is annealed in a N_2 ambient to form crystalline silicon sidewall spacers before the implant step.

21. The method of claim **12** wherein step (e) is performed by selectively patterning a photoresist layer to cover the second active region and then implanting the first active region with BF_2^+ ions at an energy between about 12 and 17 KeV and a dosage between about 5×10^{15} ions/cm^2 and 6×10^{15} ions/cm^2.

22. The method of claim **12** wherein step (f) is performed by selectively patterning a photoresist layer to cover the first active region and then implanting the second active

region with P^{31+} ions at an energy between about 10 and 30 KeV and a dosage between about 5×10^{15} ions/cm^2 and 6×10^{15} ions/cm^2.

23. The method of claim **12** wherein said rapid thermal anneal step is performed by heating the substrate in a N_2 atmosphere at a temperature between about 900^{o}C and 1100^{o}C for a period between about 7 and 13 seconds.

24. The method of claim **12** wherein forming a metal silicide layer is comprised of depositing a layer of titanium on said substrate.

25. The method of claim **24** wherein unreacted titanium is removed after the silicidation step by etching with a solution of 1:1:1 NH_4OH:H_2O_2:H_2O.

26. A MOS transistor formed on a semiconductor substrate, comprising:

(a) a substrate having isolation regions and an active region formed therebetween, said active region has an overlying gate dielectric layer and a gate electrode with two sides on the gate dielectric layer;

(b) a first sidewall spacer formed on each side of the gate electrode;

(c) a silicon sidewall spacer formed adjacent to each first sidewall spacer;

(d) a shallow source/drain region in said substrate underlying each first sidewall spacer and an adjacent silicon sidewall spacer;

(e) a deep source/drain region in said substrate between said silicon sidewall spacer and an adjacent isolation region; and

(f) a metal silicide layer on said gate electrode, over said deep source/drain regions, and on said silicon sidewall spacers, said metal silicide layer has openings over the first sidewall spacers.

27. The MOS transistor of claim **26** wherein said substrate is comprised of silicon and said isolation regions are shallow trench isolation features comprised of silicon oxide or a low k dielectric material.

28. The MOS transistor of claim **26** wherein the gate dielectric layer is comprised of silicon oxide or a high k dielectric material.

29. The MOS transistor of claim **26** wherein said gate electrode has a thickness between about 1500 and 1800 Angstroms and is comprised of polysilicon, SiGe, or SiGeC.

30. The MOS transistor of claim **26** wherein said first sidewall spacer is comprised of silicon oxide or silicon oxynitride having a width from about 150 to 200 Angstroms.

31. The MOS transistor of claim **26** wherein said silicon sidewall spacer has a maximum width of about 1500 to 1600 Angstroms.

32. The MOS transistor of claim **26** wherein said MOS transistor is a PMOS type having shallow and deep source/drain regions that are doped with a p-type impurity.

33. The MOS transistor of claim **32** wherein the p-type impurity is comprised of boron.

34. The MOS transistor of claim **26** wherein said MOS transistor is an NMOS type having shallow and deep source/drain regions comprised of an n-type impurity.

35. The MOS transistor of claim **34** wherein the n-type impurity is comprised of phosphorous.

36. The MOS transistor of claim **32** further comprised of an NMOS transistor formed adjacent to said PMOS transistor on said substrate, comprising:

(a) an active region formed between isolation regions, said active region has an overlying gate dielectric layer and a gate electrode with two sides above the gate dielectric layer;

(b) a first sidewall spacer formed on opposite sides of the gate electrode;

(c) a silicon sidewall spacer formed adjacent to each first sidewall spacer;

(d) a shallow source/drain region in said substrate underlying each first sidewall spacer and an adjacent silicon sidewall spacer;

(e) a deep source/drain region in said substrate between said silicon sidewall spacer and an adjacent isolation region; and

(f) a metal silicide layer on said gate electrode, over said deep source/drain regions, and on said silicon sidewall spacers, said metal silicide layer has openings over the first sidewall spacers..

37. The MOS transistor of claim **26** wherein said metal silicide is comprised of titanium silicide with a thickness between about 100 and 200 Angstroms.

38. The MOS transistor of claim **26** wherein said metal silicide layer is comprised of one or more of Ni, Co, W, Ta, Pt, Er, Hf, Al, and Pd.